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09/846,868	05/01/2001	Jong Chan	10980422-3	5386

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EXAMINER	
MASKULINSKI, MICHAEL C	
ART UNIT	**PAPER NUMBER**
2184	

DATE MAILED: 12/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/846,868	CHAN, JONG	
	Examiner	Art Unit	
	Michael C Maskulinski	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *1-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Non-Final Office Action

Claim Objections

1. Claims 41 and 44 are objected to because of the following informalities: in claim 41, line 7, a "salve memory device" is claimed, which should be a "slave memory device" and in claim 44, line 4, "enabling the salve control unit" is claimed, which should be "enabling the slave control unit." Appropriate correction is required.

2. Claim 48 is objected to because of the following informalities: as written, claim 48 is dependent from claim 37. This results in a lack of antecedent basis for "the disabling step." The Examiner believes that claim 48 should depend off of claim 47 in order to support "the disabling step" of claim 48 and has interpreted the claim as such. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 37-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Jung et al., U.S. Patent 6,389,554 B1.

Referring to claim 37:

a. In Figure 1 and in column 3, lines 7-12, Jung et al. teach providing a plurality of control units, each control unit having a capacity to control the transfer of data between the data processor and the data unit, each control unit having a memory device and signal paths coupled to the memory device, the signal paths enabling access to the associated memory device.

b. In column 5, lines 51-57, Jung et al. disclose a bus transceiver part for exchanging data with a CPU through a system bus and having a bus transceiver which is connected to the first memory controller and a bus transceiver to the second memory controller to thereby determine as to whether the first or second memory controller operate (selecting one of the control units as a master control unit to control transfer of data between the data processor and the data unit and designating a second one of the control units as a slave control unit).

c. In column 6, lines 6-9, Jung et al. disclose that the first memory is a general memory, in which the operating system and application program are loaded and changed data contents are stored (transferring the data between the data processor and the data unit by employing the memory device in the master control unit).

d. In column 5, lines 57-65, Jung et al. disclose a memory switch part for exchanging data between the active module and the standby module having

memory switches which set direction of memory bus in accordance with an operation mode of module (generating, in the master control unit, values for the signal paths associated with the master memory device to transfer data to the master memory device), so that write operation performed in the memory controller of the active module will be executed in the standby module with the same contents (synchronizing the memory device in the master control unit with the memory device in the slave control unit including transferring a subset of the generated signal paths to the signal paths associated with the slave memory device) and memory switch controller for controlling the memory switches (allowing the generated signals to perform the data transfer to the master memory device and the slave memory device).

Referring to claim 38, in column 5, lines 57-65, Jung et al. disclose a memory switch part for exchanging data between the active module and the standby module having memory switches which set direction of memory bus in accordance with an operation mode of module, so that write operation performed in the memory controller of the active module will be executed in the standby module with the same contents and memory switch controller for controlling the memory switches (generating, in the master control unit, values for the signal paths associated with the slave memory device that enables access to the slave memory device).

Referring to claim 39, in column 5, lines 57-65, Jung et al. disclose a memory switch part for exchanging data between the active module and the standby module having memory switches which set direction of memory bus in accordance with an

operation mode of module, so that write operation performed in the memory controller of the active module will be executed in the standby module with the same contents and memory switch controller for controlling the memory switches. Associating an address and control signal path with each memory device that enables access to the corresponding memory device comprising producing values for the address and control signal paths associated with the master memory device is inherent to the system of Jung et al. Further, transmitting the address and control signal paths associated with the master memory device to the address and control signal paths associated with the clave memory device is inherent to the system of Jung et al. because as stated above, the write operation performed in the memory controller of the active module will be executed in the standby module with the same contents.

Referring to claim 40:

a. In column 5, lines 57-58, Jung et al. disclose a memory switch part for exchanging data between the active module and the standby module (associating with the master memory device a first control signal that controls access to the slave memory device).

b. In column 5, lines 51-57, Jung et al. disclose a bus transceiver part to determine whether the first and second memory controller operate (associating with each memory device a second control signal that controls access to the corresponding memory device).

c. Producing values for the first control signal and the second control signal associated with the master memory device is inherent to the system of Jung et al.

d. In column 5, lines 63-65, Jung et al. disclose a memory switch controller for controlling the memory switches (transmitting the first control signal associated with the master memory device to the second control signal associated with the slave memory device).

Referring to claim 41, in column 5, lines 57-65, Jung et al. disclose a memory switch part for exchanging data between the active module and the standby module having memory switches which set direction of memory bus in accordance with an operation mode of module, so that write operation performed in the memory controller of the active module will be executed in the standby module with the same contents and memory switch controller for controlling the memory switches (receiving data values for the data signal path associated with the master memory device and transmitting the received data values to the data signal path associated with the slave memory device).

Referring to claim 42, in column 5, lines 63-65, Jung et al. disclose a memory switch controller for controlling the memory switches (associating with the signal paths associated with each memory device a control mechanism that enables a transfer of values from a first signal path to a second signal path). Further, in column 5, lines 57-65, Jung et al. disclose a memory switch part for exchanging data between the active module and the standby module having memory switches which set direction of memory bus in accordance with an operation mode of module, so that write operation performed

in the memory controller of the active module will be executed in the standby module with the same contents (enabling the control mechanism associated with the master memory device and the control mechanism associated with the slave memory device to transfer values between the master signal paths and the slave signal paths).

Referring to claim 43, in column 7, lines 59-67 continued in column 8, lines 1-26, Jung et al. teach disabling the control mechanism associated with a memory device to inhibit a transfer and receipt of signal path values.

Referring to claim 44, in column 7, lines 59-67 continued in column 8, lines 1-26, Jung et al. teach suspending the master control unit from controlling the data transfer between the data processor and the data unit; enabling the slave control unit to control the transfer of data between the data processor and the data unit; and transferring the data between the data processor and the data unit by employing the memory device in the slave control unit.

Referring to claim 45, in column 9, lines 61-67 continued in column 10, lines 1-3, Jung et al. disclose that if the duplexing separation is not normally formed due to generation of an unexpected trouble, the memory contents in the primary memory area are discarded and the OS stored in the secondary memory area is copied in the primary memory area, so that the system retries the operation where the trouble has occurred at the OS level to thereby prevent the two modules from being under dual down state (determining that the master control unit has experienced an operational failure).

Referring to claim 46, in column 9, lines 61-67 continued in column 10, lines 1-3, Jung et al. disclose that if the duplexing separation is not normally formed due to

generation of an unexpected trouble, the memory contents in the primary memory area are discarded and the OS stored in the secondary memory area is copied in the primary memory area, so that the system retries the operation where the trouble has occurred at the OS level to thereby prevent the two modules from being under dual down state (receiving an indication that the memory device in the master control unit has failed).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jung et al., U.S. Patent 6,389,554 B1 as applied to claim 37 above, and further in view of Kern et al., U.S. Patent 5,734,818.

Referring to claims 47 and 48, in column 9, lines 61-67 continued in column 10, lines 1-3, Jung et al. disclose that if the duplexing separation is not normally formed due to generation of an unexpected trouble, the memory contents in the primary memory area are discarded and the OS stored in the secondary memory area is copied in the primary memory area, so that the system retries the operation where the trouble has occurred at the OS level to thereby prevent the two modules from being under dual down state. However, Jung et al. don't explicitly disclose disabling the master control unit from accessing the slave memory device and suspending operation of the slave unit because the slave control unit has experienced an operational failure. In column 7,

lines 56-67 continued in column 8, lines 1-5, Kern et al. disclose that in the case that the duplex pair is in a "failed" state, then the primary storage controller notifies the primary processor that the duplex pair has suspended or failed. Further, in column 5, lines 58-67 continued in column 6, lines 1-7, Kern et al. disclose that the primary site may break the duplex pair if the primary site is unable to write updated data to the secondary site. It would have been obvious to one of ordinary skill at the time of the invention to include the detection of an error in the slave device and suspension of the device in response to the error of Kern et al. into the system of Jung et al. A person of ordinary skill in the art would have been motivated to make the modification because a failed device can corrupt data or it can cause further errors by not being accessible by the master device. Further, if the failure is in the communication link, then the primary storage controller is unable to communicate the failure directly to the secondary storage controller. Therefore, disconnection of the secondary storage controller is necessary (see Kern et al.: column 7, lines 63-66).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. 2002/0133744 A1	Oldfield et al.
U.S. Patent 6,578,158	Deitz et al.
U.S. Patent 5,202,822	McLaughlin et al.
U.S. Patent 5,088,021	McLaughlin et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (703) 308-6674. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MM

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